

What is claimed is:

- 1 1. A method comprising:
2 reading a design description for a heterogeneous reconfigurable device;
3 combining functions within the design description into groups; and
4 analyzing the groups for compliance with user-specified constraints.
- 1 2. The method of claim 1 wherein analyzing comprises estimating power
2 consumption of the groups.
- 1 3. The method of claim 1 wherein analyzing comprises estimating area
2 occupied by the groups.
- 1 4. The method of claim 1 further comprising re-combining functions into
2 groups and re-analyzing the groups for compliance with the user-specified
3 constraints.
- 1 5. The method of claim 1 wherein analyzing comprises comparing estimated
2 parameters with prioritized user-specified constraints.
- 1 6. The method of claim 1 further comprising compiling the functions to run on
2 processing elements within the heterogeneous reconfigurable device.
- 1 7. The method of claim 6 further comprising placement of the groups onto
2 particular processing elements within the heterogeneous reconfigurable device.
- 1 8. The method of claim 7 further comprising analyzing the placement for
2 compliance with user-specified constraints.

- 1 9. The method of claim 8 wherein analyzing the placement comprises
2 estimating latency.
- 1 10. The method of claim 9 wherein estimating latency comprises estimating
2 interconnect delay.
- 1 11. The method of claim 9 wherein estimating latency comprises estimating
2 processing latency.
- 1 12. The method of claim 9 wherein estimating latency further comprises
2 estimating processing latency and interconnect latency.
- 1 13. The method of claim 7 further comprising producing a file with a placed
2 design for profiling.
- 1 14. The method of claim 13 further comprising profiling the design and
2 comparing with user-specified constraints.
- 1 15. The method of claim 14 further comprising re-grouping functions in
2 response to the profiling.
- 1 16. The method of claim 14 further comprising re-performing placement in
2 response to the profiling.
- 1 17. A method comprising:
2 mapping a plurality of functions into groups;
3 placing the groups on resources within a heterogeneous reconfigurable
4 device;
5 producing a mapped and placed design representation;
6 profiling the design representation; and

7 comparing results from the profiling with user-specified constraints.

1 18. The method of claim 17 further comprising re-mapping the plurality of
2 functions into groups.

1 19. The method of claim 17 further comprising re-placing the groups on
2 resources.

1 20. The method of claim 17 wherein comparing results comprises comparing an
2 estimated latency with a latency specified in the user-specified constraints.

1 21. The method of claim 20 wherein the estimated latency includes processing
2 latency and interconnect latency.

1 22. The method of claim 17 wherein the user-specified constraints include
2 latency, power, and throughput.

1 23. An apparatus including a medium to hold machine-accessible instructions
2 that when accessed result in a machine performing:
3 reading a design description for a heterogeneous reconfigurable device;
4 combining functions within the design description into groups; and
5 analyzing the groups for compliance with user-specified constraints.

1 24. The apparatus of claim 23 wherein the machine-accessible instructions when
2 accessed further result in the machine performing:
3 re-combining functions into groups; and
4 re-analyzing the groups for compliance with the user-specified constraints.

1 25. The apparatus of claim 23 wherein the machine-accessible instructions when
2 accessed further result in the machine performing:

3 compiling the functions to run on processing elements within the
4 heterogeneous reconfigurable device.

1 26. The apparatus of claim 23 wherein analyzing comprises comparing
2 estimated parameters with prioritized user-specified constraints.

1 27. An electronic system comprising:
2 a processor; and
3 a static random access memory to hold instructions that when accessed result
4 in the processor performing reading a design description for a heterogeneous
5 reconfigurable device, combining functions within the design description into
6 groups, and analyzing the groups for compliance with user-specified constraints.

1 28. The electronic system of claim 27 wherein the instructions when accessed
2 further result in the processor performing re-combining functions into groups, and
3 re-analyzing the groups for compliance with the user-specified constraints.

1 29. The electronic system of claim 28 wherein analyzing comprises comparing
2 estimated parameters with prioritized user-specified constraints.